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(71) Applicant: **ZIPTRONIX** [US/US]; 3040 Cornwallis Road, Research Triangle Park, NC 27709 (US).

(72) Inventor: **TONG, Qin-Yi**; 3511 Meadowrun Drive, Durham, NC 27707 (US).

(74) Agent: **SCHLIER, Carl**; Oblon, Spivak, McClelland, Maier & Neustadt, P.C., 4th floor, 1755 Jefferson Davis Highway, Arlington, VA 22202 (US).

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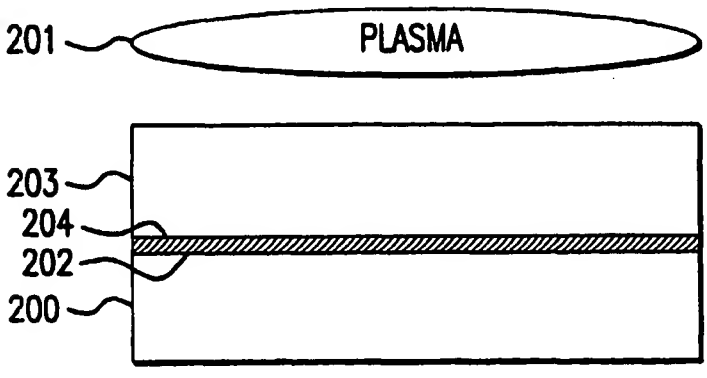
(54) Title: A METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE



(57) Abstract: A process for bonding oxide-free silicon substrate pairs and other substrates at low temperature. This process involves modifying the surface of the silicon wafers (200, 203) to create defect regions (202, 204), for example by plasma-treating the surface to be bonded with boron-containing plasmas such as a B2H6 plasma (201). The surface defect regions may also be amorphized (202, 204). The treated surfaces are placed together, thus forming an attached pair at room temperature in ambient air. The bonding energy reaches approximately 400 mJ/m2 at room temperature, 900mJ/m2 at 150 °C, and 1800 mJ/m2 at 250 °C. The bulk silicon fracture energy of 2500 mJ/m2 was achieved after annealing at 350-400 °C. The release of hydrogen from B-H complexes and the subsequent absorption of the hydrogen by the plasma induced modified layers on the bonding surfaces at low temperature is most likely responsible for the enhanced bonding energy.

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A METHOD OF EPITAXIAL-LIKE WAFER BONDING AT LOW TEMPERATURE AND BONDED STRUCTURE

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to a method of epitaxial-like bonding of wafer pairs at low temperature, and more particularly to a method of bonding in which the wafer surfaces are modified to create surface and subsurface defect areas, and possibly amorphized, by ion implantation or plasma, preferably by boron-containing ions or a plasma such as B_2H_6.

Discussion of the Background:

For many optoelectronic and electronic device applications, homo-epitaxial single crystalline layers consisting of same material with same crystalline orientation but different doping types or levels are necessary. For some device applications, active layers comprising single crystalline dissimilar materials are required. The active layers should be high crystallographic quality with interfaces that are thermally conductive and almost optical loss free. Conventional hetero-epitaxial growth techniques applied to these lattice mismatched active layers usually result in a large density of threading dislocations in the bulk of the layers. Bonding of single crystalline wafers of identical or dissimilar materials is an unique alternative approach to the epitaxial growth. Not only highly lattice-mismatched wafers can be bonded but also wafers with different crystalline orientations can be combined. Ideally, the mismatches of single crystalline bonding wafers are accommodated by dislocations (in lattice-mismatch case) or an amorphous layer (in orientation-mismatch case) localized at the bonding interface with no defects generated in the bulk area. This approach is termed expitaxial-like bonding. The epitaxial-like bonding can also be employed to prepare unique devices by integrating already processed device layers.

However, conventional epitaxial-like bonding is achieved by high temperature annealing. To bond wafers composed of thermally mismatched materials, severe and often damaging thermal stresses can be induced with high temperature annealing. Since thermal stresses can increase significantly with the size of dissimilar wafers, only small wafers currently can be epitaxially bonded at high temperatures. The high temperature annealing

process can also produce unwanted changes to bonding materials and often prevents the bonding of processed device wafers. The bonding materials may decompose at high temperatures, even if the bonding wafers are thermally matched.

In order to epitaxially bond large wafers of dissimilar materials or processed wafers, an epitaxial-like bonding interface must be achieved at or near room temperature, or one wafer of the bonded pair must be thinned sufficiently before annealing to elevated temperatures. Although Göesele et al. in Applied Physics Letters 67, 3614 (1995) and Takagi et al in Applied Physics Letters 74, 2387, 1999 reported room temperature epitaxial-like bonding of silicon wafers in ultrahigh vacuum, high temperature (>600°C) pre-annealing in the former case or high external pressure (>1 MPa) in the latter case were required to achieve the bond that may introduce undesired effects to the bonding wafers.

Recently, M. Bruel in Electronics Letters 31,1201 (1995) reported a promising generic thinning approach using a hydrogen-induced layer transfer method (so-called smart-cut method). In this approach, H atoms are implanted into a Si wafer to such concentration that a significant fraction of Si-Si bonds are broken creating a buried H-rich layer of micro-cracks susceptible to cleavage or fracture. By bonding the topmost oxide covered hydrophilic Si wafer surface to another substrate, a thin layer of the Si wafer can then be transferred by fracture of the H-rich region. However, this process requires that the bonding energy between the bonded wafers be higher than the fracture energy of the hydrogen-induced crack region at the layer transfer temperature. The layer transfer temperatures must be lower than the temperature beyond which hydrogen molecules in the material become mobile. For silicon, the temperature is about 500°C (see Chu et al in Physics Review B, 16, 3851 (1987)). The bonding energy of conventional HF dipped hydrophobic silicon wafer pairs is higher than the hydrogen-induced region only after annealing at temperatures higher than 600°C. Therefore, this process does not work for oxide-free hydrophobic silicon wafer bonding.

Typically, HF-dipped, hydrogen-terminated hydrophobic silicon wafers are used to realize epitaxial-like bonding after annealing at >700°C. In order for bonded hydrophobic silicon wafer pairs to reach bulk fracture energy, Tong et al. in Applied Physics Letters 64, 625 (1994) reported that hydrogen (from HF-dip, mainly Si-H_2 and Si-H terminated hydrophobic silicon surfaces at the bonding interface) must be removed so that strong Si-Si epitaxial bonds across the mating surfaces can be formed. The reaction is illustrated in

Equation (1).

$$Si\text{-}H + H\text{-}Si \rightarrow Si\text{-}Si + H_2 \quad (1)$$

The release of hydrogen from a stand-alone silicon wafer dipped in HF was demonstrated to start at about 367 °C from Si-H_2 and 447 °C from Si-H in an ultrahigh vacuum. Since hydrogen molecules become mobile in silicon only at temperatures higher than 500°C, annealing at temperatures higher than 700°C have been found necessary to completely deplete hydrogen from the bonding interface that results in a high bonding energy. Therefore, the smart-cut method for a layer transfer using conventional HF-dipped silicon wafer pairs is not possible because the bonding energy is too low at layer transfer temperatures that are lower than 500 °C.

Based on above arguments, it becomes clear that the development of a low temperature epitaxial-like wafer bonding technology that is both cost-effective and manufacturable is essential for many advanced materials and device applications.

SUMMARY OF THE INVENTION

Accordingly, one object of this invention is to provide a wafer bonding method and bonded structure in which epitaxial-like bonding is achieved at near room temperature in ambient conditions without an external pressure.

Another object of this invention is to provide a wafer bonding method and bonded structure using bonding surfaces treated to obtain amorphized or partially amorphized surfaces by ion implantation or plasma, preferably by boron-containing ions or plasma.

These and other objects of the present invention are provided by a method for bonding first and second substrates including steps of preparing substantially oxide-free first and second surfaces of respective first and second substrates, creating a surface defect region in each of said first and second surfaces, and bonding said first and second surfaces. Creating the defective region may include plasma-treating the first and second surfaces of the first and second substrates with a plasma, and preferably a boron-containing plasma. The plasma-treating step may utilize a plasma in reactive ion etch (RIE) mode using B_2H_6 gas, and possibly a mixture of B_2H_6, He, and Ar gases. Other gas plasmas, such as Armay also be used.

As a result of the plasma-treating step, a thin amorphous layer may be formed in the

first and second surfaces. A monolayer of boron may also be on said first and second surfaces and first and second surfaces may be doped with boron when a boron-containing plasma is used. Also, a few monolayers of boron are introduced into each of the first and second surfaces during said plasma-treating step.

After contacting, the substrates are maintained in contact, preferable under low vacuum but also in ambient air. A bonding energy of about 400 mJ/m^2 may be obtained at room temperature. Also, when the bonded pair of substrates is maintained at a temperature no more than about 250°C after contacting, a bond strength of at least about 1500 mJ/m^2 may be obtained, and a bonding energy of about 2500 mJ/m^2 (bulk silicon fracture energy) may be obtained at 350 °C. The method may also include step of annealing said bonded first and second surfaces at a temperature in the range of about 250-450 °C, or at a temperature not exceeding about 350°C. A substantial portion of said amorphous layers in said first and second surfaces may be recrystallized, possibly in a separate annealing step.

The creating step may also include ion-implanting the first and second surfaces. As or B may be used to implant the surfaces. In the case of B, a surface layer is formed on the surface of the substrate and the energy of the implant is chosen to place the peak of the concentration profile at approximately the interface between the substrate surface and the surface layer. In the case of As, the surface is directly implanted and a thicker amorphous layer may be formed.

After contacting, the implanted substrates are maintained in contact, preferable under low vacuum but also in ambient air. The bonded pair may be heated at a temperature no more than about 400°C. The bonded pair of substrates may be maintained at a temperature no more than about 400°C after contacting. A bonding energy of about 2500 mJ/m^2 (bulk silicon fracture energy) may be obtained.

To obtain the substantially oxide-free surfaces, the substrates may be immersed in a first etching solution, such as a hydrofluoric acid solution, before said plasma-treating step, and immersed in a second etching solution, such as a hydrofluoric acid solution, after said plasma-treating step. The substrates may be cleaned before immersing in the first etching solution, preferably using an RCA-1 solution.

The method may also include plasma treating an exposed surface of the bonded pair of substrates in a boron-containing plasma, and bonding a third wafer to said exposed surface.

The method may also include creating the defect region or amorphous layer in the surface of a silicon layer formed on a semiconductor device wafer. Two or more of the treated wafers may be bonded together.

The first and second substrates may be selected from Si, InGaAs, InP, GaAs, Ge, SiC and other semiconductors.

The objects of the invention may also be achieved by a method including amorphization of first and second surfaces of first and second silicon substrates by ion implantation or plasma, and contacting the first and second surfaces to form a bonded pair of substrates. The substrates may be immersed in a first hydrofluoric acid solution before said amorphization step, and immersed in a second hydrofluoric acid solution after said amorphization step by plasma. The substrates may be cleaned before immersing in the first hydrofluoric acid solution, preferably using an RCA-1 solution. The amorphization step may utilize arsenic (As) ion implantation or argon (Ar) RIE plasma.

After contacting, the substrates are maintained in contact, preferable under low vacuum but also in ambient air. The bonded pair may be heated at a temperature no more than about 400°C. The bonded pair of substrates may be maintained at a temperature no more than about 400°C after contacting. A bonding energy of about 2500 mJ/m^2 (bulk silicon fracture energy) may be obtained. The bonded amorphous layers at the bonding interface can be completely recrystallized after annealing at 450°C.

The objects of the invention may also be achieved by a bonded structure having a first substrate having a first surface, a first amorphous layer formed in the first surface, and a second substrate having a second surface, a second amorphous layer formed in the second surface. The first surface is bonded to the second surface to form a bonded pair of substrates.

One of said first and second substrates of said bonded pair may have a third surface with an amorphous layer. A third substrate having a fourth surface, with a fourth amorphous layer formed in said fourth surface may be bonded to the bonded pair.

The first and second surfaces may comprise a surface exposed to boron-containing plasma. One of the first and second substrates of the bonded pair may have a planar surface exposed to boron-containing plasma bonded to a third surface of a third substrate exposed to boron-containing plasma. The first, second and third substrates may be selected from Si, InGaAs, InP, GaAs, Ge, SiC and other semiconductors.

The first and second substrates may comprise respective first and second semiconductor devices, the first surface may comprise a substantially planar surface of a first silicon layer formed on the first device, and the second surface may comprise a substantially planar surface of a second silicon layer formed on the second device.

The first surface may comprise a first silicon surface exposed to an inert gas plasma, and the second surface may comprise a second silicon surface exposed to an inert gas plasma.

The first surface may comprise a first silicon surface implanted with boron, and the second surface may comprise a second silicon surface implanted with boron.

The first surface may comprise a first silicon surface implanted with arsenic, and the second surface may comprise a second silicon surface implanted with arsenic.

The bonded structure according to the invention may include a first substrate having an amorphized first surface and containing boron and a second substrate having an amorphized second surface and containing boron, with the first surface being bonded to the second surface to form a bonded pair of substrates. The first and second substrates may be selected from Si, InGaAs, InP, GaAs, Ge, SiC and other semiconductors.

The first surface may comprise a first silicon surface exposed to a boron-containing plasma, and the second surface may comprise a second silicon surface exposed to a boron-containing plasma.

The first surface may comprises a first silicon surface implanted with boron, and the second surface may comprise a second silicon surface implanted with boron.

The bonded structure may also have a first substrate having a first surface implanted with boron, and a second substrate having a second surface implanted with boron. The first surface is bonded to said second surface to form a bonded pair of substrates. One of the first and second substrates of the bonded pair may have a planar surface implanted with boron. A third surface, implanted with boron, of a third substrate may be bonded to the planar surface. The first, second and third substrates may be selected from Si, InGaAs, InP, GaAs, Ge, SiC and other semiconductors.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the

following detailed description when considered in connection with the accompanying drawings, wherein:

FIG. 1 is a flow chart illustrating method steps of the present invention;

FIGS. 2A-2E are sectional diagrams illustrating a first embodiment of the method according to the invention, and a bonded structure according to the invention;

FIG. 3 is graph depicting room temperature bonding energy as a function of storage time of bonded pairs of B_2H_6 treated hydrophobic silicon wafers;

FIG. 4 is a graph depicting bonding energy as a function of annealing temperature of B_2H_6 treated, boron-implanted treated, Ar plasma treated, and conventional hydrophobic (HF dipped only) silicon wafer pairs;

FIG. 5 is a graph depicting bonding energy as a function of annealing time at 250°C for B_2H_6 treated wafer pairs;

FIG. 6 is a schematic of surface terminations on B_2H_6 plasma treated and HF dipped silicon wafers;

FIG. 7 is a flow chart showing a second embodiment of the method according to the present invention;

FIGS. 8A-8C are sectional diagrams illustrating a second embodiment of the method according to the invention, and a bonded structure according to the invention;

FIG. 9 is a graph depicting bonding energy as a function of annealing temperature;

FIG. 10 is an TEM (Transmission Electron Microscopy) image of an As-implanted amorphous-Si/amorphous-Si (a-Si/a-Si) bonding interface;

FIG. 11 is a HRTEM (High Resolution TEM) image of an As-implantation induced amorphous layer in a bonding wafer;

FIG. 12 is a HRTEM image for an As-implanted bonded pair after annealing;

FIG. 13 is a graph depicting bonding energy as a function of annealing temperature of B_2H_6 treated InP/InP wafer pairs;

FIG. 14 is a graph depicting bonding energy as a function of annealing temperature of B_2H_6 treated Si/InP wafer pairs;

FIGS. 15A-15C are diagrams of a forming a bonded structure according to the invention; and

FIGS. 16A-16E are diagrams of a forming a bonded structure according to the

invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, wherein like reference numerals designate identical or corresponding parts throughout the several views, and more particularly to FIG. 1 thereof, FIG. 1 shows method steps of the present invention. In step 100, the substrates are cleaned using, for example, a wet RCA-1 ($H_2O+H_2O_2+NH_4OH$) solution. Other cleaning methods are possible, such as $H_2SO_4+H_2O_2$ or dry clean. Following the cleaning step using the RCA-1 solution, the substrates are immersed in step 101 in a hydrofluoric acid aqueous solution such as 1%HF solution to remove the surface thin native oxide layer. Upon removal from the hydrofluoric acid solution, the surfaces of the substrates are modified by creating surface and/or subsurface damage areas by ion implantation or plasma, preferably using boron-containing ions or boron-containing plasma, in step 102. By subsurface, it is meant at least the layer of atoms below the surface layer. The treatment may approach or reach amorphization to form a thin amorphous layer may be formed in the surface of the substrates. The surface treatment, when using boron, may introduce boron into the substrate surface.

Upon termination of the treatment, the substrates in step 103 are immersed in a dilute hydrofluoric acid aqueous solution such as 1%HF solution to remove the surface thin native oxide layer or any other oxide formed on the surface. Surfaces of the substrates which were treated in step 103 are placed together in step 104 at room temperature in atmosphere and form a room temperature bonded substrate pair. The attached substrate pair is preferably placed inside a low vacuum system, but may also be placed in ambient. The bonded pair is then annealed at low temperatures in step 105. The temperature may be selected to recrystallize the thin amorphous layers formed during the ion implantation or plasma treatment. Recrystallization may also be carried out in a separate annealing procedure. The wafer bonding method of the present invention achieves high bonding energy near room temperature.

FIGS. 2A-2E show sectional views of the first embodiment of the method according to the invention. In FIG. 2A, a substrate 200, after immersing in the aqueous HF solution, is exposed to a plasma 201. FIG. 2B illustrates wafer 200 after the plasma treatment. The plasma modifies the surface 202 of the wafer to create defect areas and possibly a thin

amorphous layer. Subsurface (the layer adjacent the surface) defect areas may also be formed. Surface 202 is drawn with a heavier line to illustrate the defective area or amorphous layer formed by the plasma treatment. The amorphous layer formed is about a few nm or more in thickness. In a preferred case, the plasma is a boron-containing plasma and, most preferably, a B_2H_6 plasma. The position of the B in the surface structure will be described below in connection with FIG. 6.

The wafer is immersed in the aqueous HF solution as described above. Another wafer 203 having a similarly plasma treated surface 204 is placed in contact with wafer 200 with surfaces 202 and 204 directly contacted to form the bonded structure at room temperature in FIG. 2C. The bonded structure is annealed at a low temperature and is then ready for further processing, such as low-temperature annealing, substrate lapping, device formation, etc., or a combination of processes. The process may be continued by plasma-treating the exposed surface 205 of wafer 203 (FIG. 2D) and bonding it to another plasma-treated surface 207 of wafer 206 (FIG. 2E). Any number of substrates may be bonded together.

EXAMPLE

75 mm diameter, 1-10 ohm-cm, p-type Si (100) substrate wafers were used. The wafers were cleaned in a RCA-1 solution, dipped in a 1% hydrofluoric aqueous solution followed by treatment in B_2H_6 plasma for an appropriate time period depending on the plasma system used. Appropriate plasma treatment times have ranged from 30 sec. to 5 min. The B_2H_6 plasma treatment consisted of a mixed gas of 20 sccm of 0.5% B_2H_6/99.5% He and 20 sccm Ar in an inductor coupled plasma (ICP) operating in a reactive ion etch mode with a RF power of 38 W at a pressure of ~5 mTorr. A ~100 V self-biased voltage was generated. This self-bias is the lowest possible self-bias for a stable plasma treatment in the plasma treatment system used herein. The wafers were then dipped in a diluted 1% HF solution to remove any oxide on the wafer surfaces. The wafers were then placed together without water rinse and bonded in air at room temperature.

The bonded wafer pair was stored in a low vacuum chamber at a vacuum level of about, for example, 700 Pa. The vacuum level is not critical. The bonding energy (specific surface energy) of the bonded pairs was determined by measuring the crack length introduced by inserting a razor blade into the bonding interface to partially separate the two wafers. FIG.

3 shows the room temperature bonding energies as a function of storage time for B_2H_6 plasma-treated hydrophobic bonded silicon wafers. Compared with a typical room temperature bonding energy of ~10-20 mJ/m^2 for conventional HF-dipped silicon wafer pairs, the bonding energy of ~400 mJ/m^2 for the B_2H_6 treated pairs is remarkably higher. A few interface bubbles were formed during low vacuum storage at room temperature, which supports the latter explanation that hydrogen released from the bonding interfaces is responsible for the increase of bonding energy at room temperature.

Bonding energy as a function of annealing temperature of B_2H_6 treated, boron-implanted treated, Ar plasma treated, and conventional hydrophobic (HF dipped only) silicon wafer pairs is shown in FIG. 4. It is important to note that for the B_2H_6 plasma treated samples, the bonding energy was ~900 mJ/m^2 at 150°C and ~1800 mJ/m^2 at 250°C, and reaches the fracture energy of bulk silicon ~ 2500 mJ/m^2 at 350°C. For comparison, FIG. 4 also shows the bonding energy as a function of annealing temperature of conventional HF dipped silicon wafer pairs. TEM (Transmission Electron Microscopy) measurements have shown that the expitaxial bonding interface in the Si/Si bonded pairs was realized after 350°C annealing.

A typical example of bonding energy as a function of annealing time at 250°C is shown in FIG. 5. The bonding energy increases quickly with annealing time and is saturated after ~20 h annealing at 250°C. A few bubbles were generated during annealing indicating that the increase in bonding energy is associated with the release of hydrogen at the bonding interface.

The B_2H_6 plasma treatment of present invention places boron not only on the surface but also in subsurface layers due to the self-bias voltage. After the HF dip, in addition to Si-H_2, Si-H and Si-F surface terminations, the B_2H_6 plasma-treated silicon surfaces will likely be terminated by Si-B:H from top surface boron atoms forming Si-B groups, by Si-B-H groups by boron at the first surface layer, and by Si-H and Si-H_2 groups that have subsurface boron atoms terminated to the silicon atoms, see FIG. 6. The bonding interface between the silicon wafer pair is most likely bridged by HF molecules resulting from the HF dip that can be removed by storage in low vacuum or in ambient at room temperature.

Since B-H complexes are very weakly polarized due to their similar electronegativity, the following reactions at the bonding interface are likely responsible for the increase in

bonding energy at room temperature:

$$Si\text{-}B{:}H + H{:}B\text{-}Si \rightarrow Si\text{-}B\text{-}B\text{-}Si + H_2 (2)$$

$$Si\text{-}B\text{-}H + H\text{-}B\text{-}Si \rightarrow Si\text{-}B\text{-}B\text{-}Si + H_2 (3)$$

The removal of hydrogen terminations on the boron atoms leads to a Si-B-B-Si bridging bond attaching one substrate to another. Moreover, as reported by Kim et al. in Applied Physics Letters 69, 3869 (1996), subsurface boron in the second layer weakens the surface Si-H bond. Hydrogen desorption from the bonding surfaces of B_2H_6 treated silicon wafers can take place at low temperatures resulting in a silicon covalent bond formation across the interface between the substrates as shown by the following reaction:

$$Si\text{-}H + H\text{-}Si \rightarrow Si\text{-}Si + H_2 (4)$$

The boron-assisted reaction completely depletes hydrogen from the bonding interface at temperatures of 350-400°C which is lower than a 700°C temperature which is required for conventional HF dipped silicon substrate bonding, when no boron is present.

In a second embodiment, an inert gas plasma is used to create the defective area and thin amorphous layer. The third embodiment preferably uses an Ar-only plasma treatment to enhance the bonding energy at low temperatures, also shown in FIG. 4. Method steps for an Ar-only plasma treatment bonding process follow all the steps shown in FIG. 1. After cleaning in RCA1 solution (step 100), silicon wafers are dipped in 1%HF solution to remove the native oxide layer of any other oxide layer (step 101). The wafers are placed in the RIE plasma system and treated with Ar plasma in 30-100 mtorr for 15 seconds to 20 minutes. Ar plasma is generated by applying a RF power from 80-200 W at 13.56 MHz (step 102). The surface self-bias voltage is in the range of 200 V to 400 V. These Ar plasma treated wafers are dipped in 1%HF to remove any surface oxide layer (step 103) and bonded at room temperature in air (step 104). After storage in low vacuum for ~20 hrs (step 105), the bonded pairs are annealed. The bonding energy reaches the bulk silicon fracture energy (2500 mJ/m^2) at 400°C. The bonding energy enhancement is likely due to that the amorphous layer formed by the Ar plasma treatment readily absorbs the hydrogen released from surface $Si\text{-}H_2$ and Si-H groups that takes place at about 300°C. The amorphous layer at the bonding interface may be recrystallized at low temperatures. Ar-only plasma treatment to enhance low temperature epitaxial-like bonding is especially attractive for applications that requires no monolayers of

boron at the bonding interface.

A third embodiment of the present invention (shown in FIG. 7) is to use ion implantation to place boron onto the surfaces of bonding substrates. In step 700, the substrates are covered by a masking layer, preferably an oxide layer. The substrates are cleaned using, for example, a wet RCA-1 solution and dried. in step 701. Surfaces of the substrates are implanted with boron using BF_3 as shown in step 702 to place the boron concentration peak at the oxide/silicon interface. As an example, forming an 800 Å thick thermal oxide on silicon wafers, boron implantation at an energy of 20 keV with a dose of $5x10^{14}/cm^2$ places boron concentration peak of $6x10^{19}/cm^2$ at the oxide/silicon interface. Employing a 6700 Å thick thermal oxide on silicon wafers, boron implantation at an energy of 180 keV with a dose of $5x10^{14}/cm^2$ places boron concentration peak of $2.5x10^{19}/cm^2$ at the oxide/silicon interface.

Following boron implantation, the substrates in step 703 are immersed in a dilute hydrofluoric acid solution to remove the oxide layer. Surfaces of the substrates which were boron-implanted in step 702 are bonded at room temperature in step 704. The attached pair is preferably placed inside a low vacuum system and annealed in air at low temperature in step 705.

Boron implantation in bonding silicon wafers can achieve the bulk silicon fracture energy at ~400°C. The bonding energy enhancement at room temperature seen with the boron plasma treated wafers is not achieved. Instead, a significant increase in bonding energy is seen at temperatures above than 300°C , as shown in FIG. 4. It is likely that lower boron concentrations on the wafer surfaces for the boron implantation treatment in comparison to the plasma treatment case delays bonding enhancement until higher annealing temperatures are used.

Released hydrogen shown in equation (4) can build an internal pressure that offsets the bonding strength at the bonding interface. In order to alleviate the internal gas pressure, released hydrogen molecules need to be removed from the interface. The plasma or ion implantation treatment according to the invention induces a defective surface layer towards amorphization providing hydrogen trapping sites. Plasma or ion implantation treatments using other gases containing boron are expected to work as well.

FIGS. 8A-8C show cross sectional views of the third embodiment of the method.

Ions 801 are implanted into a wafer 800 having a masking film 805, such as SiO_2, formed on the surface, as shown in step 8A. The masking film 805 allows the energy of the implant to be adjusted so that the peak of the concentration distribution is at the surface of wafer 800. As shown in FIG. 8B, the wafer 800 has a modified surface 802 (shown with heavier line for illustrative purpose only) after removing the masking layer by immersing in an aqueous HF solution, in the case of layer 305 being SiO_2. Another wafer 803 similarly treated with a modified surface 804 is placed in contact with wafer 800 at room temperature. The bonding of the two wafers is allowed to enhance with low-temperature annealing, as discussed above.

A fourth embodiment of the present invention is to use As (arseniic) ion implantation to silicon wafers to form an amorphous layer on the wafer surface. Method steps for an As ion implantation treatment bonding process follow the steps shown in FIG. 1. After cleaning and removing any oxide layer, As ion implantation is performed at an energy of 180 keV with a dose of $9x10^{14}/cm^2$. The As doping concentration peak of $8x10^{19}/cm^3$ is located at ~1150 Å from the silicon surface. Although this implantation induced a very low As doping on the wafer surface, an amorphous layer with 1650 Å thick was formed as confirmed both by a Monte Carlo simulation and TEM measurement (FIG. 10). The thickness of the amorphous layer can vary and is not limited to the value of this example. For instance, other ions may be implanted to create the amorphous layer. Arsenic is a dopant, and there are applications when it is desired not to dope the substrate so another ion, such as a non-doping ion like Ar, would be chosen.

After an HF dip to remove any oxide on the implanted surfaces, the wafers are bonded at room temperature in ambient conditions. After storage in low vacuum for ~20 h the bonded pairs are annealed in air. The bonding energy as a function of annealing temperature is shown in Fig. 9. The bonding energy reaches the bulk silicon fracture energy (2500 mJ/m^2) at 400°C. Bonded pairs of the As implanted silicon wafers that were annealed at 900°C to fully recrystallize the amorphous layers before bonding have shown the same bonding energy of ~400 mJ/m^2 as the conventional HF dipped Si/Si pairs after 400°C annealing. It is clear that as in the Ar plasma treatment case, the amorphous layers rather than As doping at the bonding interface play a key role in enhancing bonding energy at low temperatures.

FIGS. 10-12 show TEM images of the As-implanted substrates, and As-implanted bonded substrate pairs. In FIG. 10, a TEM image of bonding interface between the

amorphous silicon layers (a-Si/a-Si) that were formed by As implantation is shown. FIG. 11 shows an HRTEM image of the interface between the amorphous silicon and the crystal silicon substrate (a-Si/c-Si). The amorphous layer is reduced to 100 Å in thickness after annealing for 24 hours at 450°C, as shown in FIG. 12.

The above methods can be applied to other substrate combinations involving materials such as InP, GaAs, Ge, SiC, etc. Using the B_2H_6 plasma treatment process described in the first embodiment to InP/InP epitaxial-like wafer bonding, the bonding energy of the bonded InP/InP pairs reached the (100) InP bulk fracture energy of ~ 600 mJ/m^2 after annealing at 200°C for 24 h. FIG. 13 shows the bonding energy as a function of annealing temperature of the B_2H_6 treated InP/InP wafer pairs. For comparison, the bonding energy as a function of annealing temperature of conventional HF dipped InP/InP pairs is also shown.

The similar results were obtained for bonding a silicon wafer to an InP wafer. Using the B_2H_6 plasma treatment process described in the first embodiment to Si/InP epitaxial-like wafer bonding, the bonding energy of the bonded Si/InP pairs reached the (100) InP bulk fracture energy of ~ 600 mJ/m^2 after annealing at 200°C for 24 h. FIG. 14 shows the bonding energy as a function of annealing temperature of the B_2H_6 treated Si/InP wafer pairs. For comparison, the bonding energy as a function of annealing temperature of conventional HF dipped Si/InP pairs is also shown

Two or more wafers having a silicon layer formed on the surface may also be bonded, as shown in FIGS. 15A - 15C. Silicon layer 1502 of substrate 1500 is exposed to plasma 1503 in FIG. 15A. A similarly treated surface 1505 of wafer 1504 is placed in contact with surface 1502 and bonded (FIG. 15B). Surface 1505 may also be ion-implanted. The exposed surface of substrate 1504 may also be exposed to a plasma and bonded with treated surface 1507 of wafer 1506 to form a three-substrate bonded structure, as shown in FIG. 15C. These wafers may be processed wafers having devices and/or circuits formed therein with the silicon layer formed after device and/or circuit formation. The silicon layer should be planar, and may be planarized using techniques such as CMP. The silicon layer is treated using a plasma or ion-implantation, as discussed above. This structure preferably used the boron-containing plasma or boron implantation. Also, unique device structures such as double-sided power diodes, pin photodiodes and avalanche photodiodes may be realized. While the above embodiments are directed to substrates, it should be understood that a substrate may be

of varying thickness. In other words, thin substrates may be bonded to other substrates, or bonded with two substrates to be between the substrates. A bonded substrate may also be thinned to a desired thickness by lapping or polishing, as discussed above. FIGS. 16A-16E illustrate this. The surface of substrate 1600 is exposed to plasma 1601 to form treated surface 1602 (FIGS. 16A and 16B). Surface 1602 has a surface defect region and may be amorphized. Another substrate 1603 with a treated surface 1604 is bonded to surface 1602 (FIG. 16B). In FIG. 16C, a portion of substrate 1603 is removed by lapping, polishing, etc. to leave portion 1605 with surface 1606. Surface 1606 may then be exposed to a plasma (FIG. 16D) and another wafer 1607 with treated surface 1608 may be bonded to surface 1606 (FIG. 16E). Unique structures where different materials of desired thicknesses may be bonded and formed according to the invention.

Some advantages of the wafer-bonding process of the present invention are that the process utilizes manufacturable steps which bond wafers at room temperature in ambient air and annealed at temperatures no higher than 450°C to reach an epitaxial-like bond. Pre-annealing at elevated temperatures, external pressure, or high vacuum to achieve a high bonding energy are not required. The process uses common RIE plasma treatments or ion implantation that are economic, convenient and easy to implement.

In addition to the epitaxial-like wafer bonding for materials combination for preparing advanced devices such as pin and avalanche photodiodes, the process shown here can have applications in bonding unique device structures such as bonding back sides of two fully processed power devices to form double-sided power devices, can allow the device layer transfer onto carrier substrates with an epitaxial-like interface, and can be used to transfer device layers to more thermally conductive materials thus enhancing thermal management.

Numerous other modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the present invention may be practiced otherwise than as specifically described herein.

Claims:

1. A method for bonding first and second substrates, comprising:

preparing substantially oxide-free first and second surfaces of respective first and second substrates;

creating a surface defect region in each of said first and second surfaces; and

bonding said first and second surfaces.

2. A method as recited in claim 1, wherein said creating step comprises:

forming an amorphous layer about a few nm or more in thickness in each of said first and second surfaces.

3. A method as recited in claim 2, comprising:

forming said amorphous layer using one of ion implantation and plasma treatment.

4. A method as recited in claim 3, comprising:

forming said amorphous layer using As implantation.

5. A method as recited in claim 2, comprising:

forming said amorphous layer using a boron-containing plasma.

6. A method as recited in claim 5, comprising:

forming said amorphous layer using a B_2H_6 plasma.

7. A method as recited in claim 2, comprising:

forming said amorphous layer using an inert gas plasma.

8. A method as recited in claim 7, comprising:

forming said amorphous layer using an Ar plasma.

9. A method as recited in claim 2, comprising:

annealing said bonded first and second surfaces at a temperature in the range of about 250-450°C.

10. A method as recited in claim 9, comprising:

recrystallizing a substantial portion of said amorphous layers in said first and second surfaces.

11. A method as recited in claim 2, comprising:

annealing said bonded first and second surfaces at a temperature not exceeding about 350°C.

12. A method as recited in claim 1, wherein said creating step comprises:

plasma treating said first and second surfaces using a boron-containing plasma.

13. A method as recited in claim 12, comprising:

forming monolayers of boron on said first and second surfaces.

14. A method as recited in claim 12, comprising:

doping said first and second surfaces with boron.

15. A method as recited in claim 1, comprising:

bonding said first and second surfaces at room temperature.

16. A method as recited in claim 15, comprising:

annealing said bonded first and second surfaces at a temperature in the range of about 250-450°C.

17. A method as recited in claim 1, comprising:

forming said defect region using one of ion implantation and plasma treatment.

18. A method as recited in claim 1, comprising:

forming said defect region using As implantation.

19. A method as recited in claim 1, comprising:

forming said defect region using a boron-containing plasma.

20. A method as recited in claim 19, comprising:

forming said defect region using a B_2H_6 plasma.

21. A method as recited in claim 1, comprising:

forming said defect region using an inert gas plasma.

22. A method as recited in claim 21, comprising:

forming said defect region using an Ar plasma.

23. A method as recited in claim 1, comprising:

preparing substantially oxide-free first and second surfaces of respective first and second substrates made of one of Si, InP, SiC, Ge and GaAs.

24. A method as recited in claim 1, comprising:

preparing a substantially oxide-free silicon substrate having said first surface; and

preparing a substantially oxide-free substrate made of one of InP, SiC, Ge and GaAs having said second surface.

25. A method as recited in claim 1, comprising:

forming a layer of a desired thickness said first surface;

ion implanting said first surface through said layer to create said surface defect region in said first substrate; and

creating said surface defect region in said second substrate using one of ion implantation and plasma treatment.

26. A method as recited in claim 1, comprising:

creating said surface defect region in said first substrate using plasma treatment; and

creating said surface defect region in said second substrate using one of ion implantation and plasma treatment.

27. A method as recited in claim 1, comprising:

forming a silicon layer on a substrate containing a first active device as said first substrate; and

forming a silicon layer on a substrate containing a second active device as said second substrate.

28. A method as recited in claim 1, comprising:

immersing said first and second substrates in a first oxide etching solution before said creating step; and

immersing said first and second substrates in a second oxide etching solution after said creating step.

29. A method as recited in claim 28, comprising:

cleaning said first and second substrates before immersing said substrates in said first oxide etching solution.

30. A method as recited in claim 29, wherein said cleaning step comprises cleaning said first and second substrates in an RCA-1 solution.

31. A method as recited in claim 1, comprising:

forming at least one of boron-boron and Si covalent bonds between said first and second substrates.

32. A method as recited in claim 1, further comprising:

placing the bonded pair of substrates under vacuum.

33. A method as recited in claim 1, wherein said first and second substrates are

selected from Si, InGaAs, InP, GaAs, Ge and SiC.

34. A method as recited in claim 1, comprising:

creating a surface defect region in an exposed surface of said bonded pair of substrates and in a third surface of a third wafer; and

bonding said third surface to said exposed surface.

35. A method as recited in claim 1, comprising:

maintaining said bonded pair at room temperature; and

obtaining a bond strength of at least about 400 mJ/m^2.

36. A method as recited in claim 1, comprising:

maintaining said bonded pair at a temperature no more than about 400°C; and

obtaining a bond strength of at least about 1500 mJ/m^2.

37. A method as recited in claim 36, comprising:

obtaining a bond strength of at least about 2500 mJ/m^2.

38. A method for bonding first and second substrates, comprising:

forming a surface layer on respective first and second surfaces each of said first and second substrates;

ion implanting an impurity into said first and second substrates with a peak concentration of said impurity located at approximately respective interfaces between said first and second surfaces and said surface layer;

removing said surface layer from each of said first and second substrates; and

bonding said first and second surfaces.

39. A method as recited in claim 38, wherein said ion implanting step comprises:

forming a thin amorphous layer in each of said first and second surfaces.

40. A method as recited in claim 38, comprising:

forming said amorphous layer using B implantation.

41. A method as recited in claim 38, comprising:

annealing said bonded first and second surfaces at a temperature in the range of about 250-450°C.

42. A method as recited in claim 38, comprising:

recrystallizing a substantial portion of said amorphous layers in said first and second surfaces.

43. A method as recited in claim 38, comprising:

forming a surface defect region in each of said first and second surfaces.

44. A bonded structure, comprising:

a first substrate having a first surface, a first amorphous layer formed in said first surface; and

a second substrate having a second surface, a second amorphous layer formed in said second surface;

said first surface being bonded to said second surface to form a bonded pair of substrates.

45. A structure as recited in claim 44, comprising:

one of said first and second substrates of said bonded pair having a third surface, said third surface having an amorphous layer;

a third substrate having a fourth surface, a fourth amorphous layer formed in said fourth surface; and

said third surface bonded to said fourth surface.

46. A structure as recited in claim 44, wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge and SiC.

47. A structure as recited in claim 44, wherein:

said first and second substrates each comprises a silicon substrate; and

said first and second surfaces each comprises a silicon surface.

48. A structure as recited in claim 44, wherein:

said first and second substrates comprise respective first and second semiconductor devices;

said first surface comprises a substantially planar surface of a first silicon layer formed on said first device; and

said second surface comprises a substantially planar surface of a second silicon layer formed on said second device.

49. A structure as recited in claim 44, wherein:

said first surface comprises a first silicon surface exposed to a boron-containing plasma; and

said second surface comprises a second silicon surface exposed to a boron-containing plasma.

50. A structure as recited in claim 44, wherein:

said first surface comprises a first silicon surface exposed to an inert gas plasma; and

said second surface comprises a second silicon surface exposed to an inert gas plasma.

51. A structure as recited in claim 44, wherein:

said first surface comprises a first silicon surface implanted with boron; and

said second surface comprises a second silicon surface implanted with boron.

52. A structure as recited in claim 44, wherein:

said first surface comprises a first silicon surface implanted with arsenic; and

said second surface comprises a second silicon surface implanted with arsenic.

53. A structure as recited in claim 44, comprising:

at least one of boron-boron and Si covalent bonds formed between said first and second substrates.

54. A bonded structure, comprising:

a first substrate having an amorphized first surface and containing boron;

a second substrate having an amorphized second surface and containing boron; and

said first surface being bonded to said second surface to form a bonded pair of substrates.

55. A structure as recited in claim 54, wherein said first and second substrates are selected from Si, InGaAs, InP, GaAs, Ge, SiC.

56. A structure as recited in claim 54, wherein:

said first surface comprises a first silicon surface exposed to a boron-containing plasma; and

said second surface comprises a second silicon surface exposed to a boron-containing plasma.

57. A structure as recited in claim 54, wherein:

said first surface comprises a first silicon surface implanted with boron; and

said second surface comprises a second silicon surface implanted with boron.

58. A structure as recited in claim 54, comprising:

forming at least one of boron-boron and Si covalent bonds between said first and second substrates.

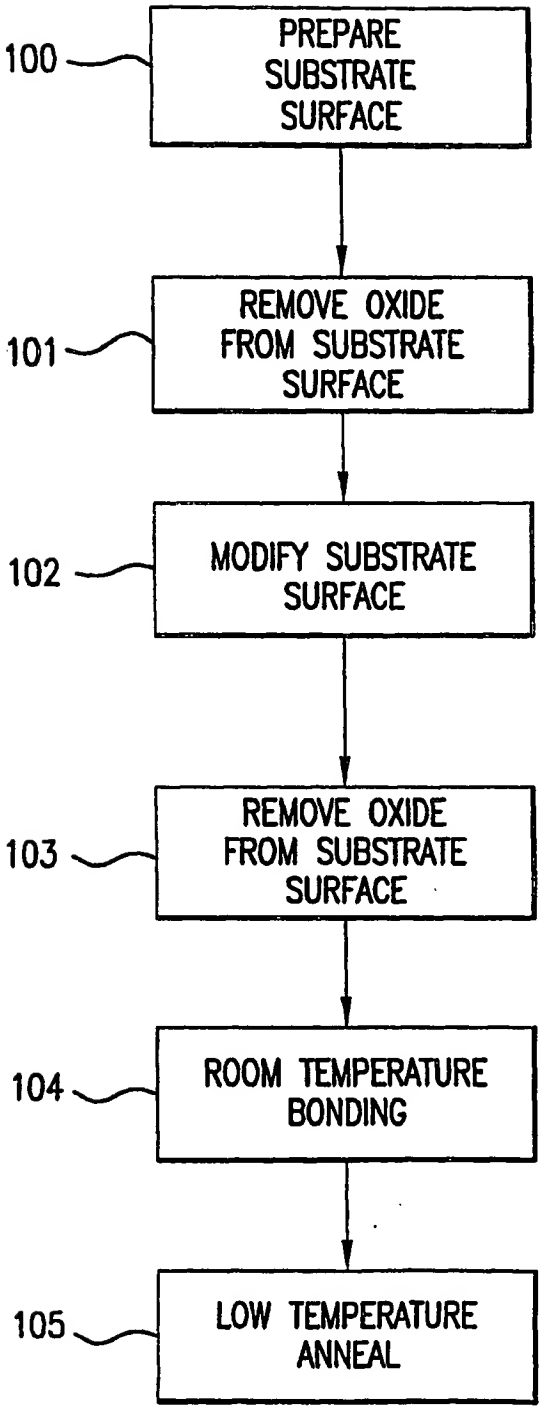

100
PREPARE SUBSTRATE SURFACE
101
REMOVE OXIDE FROM SUBSTRATE SURFACE
102
MODIFY SUBSTRATE SURFACE
103
REMOVE OXIDE FROM SUBSTRATE SURFACE
104
ROOM TEMPERATURE BONDING
105
LOW TEMPERATURE ANNEAL

FIG.1

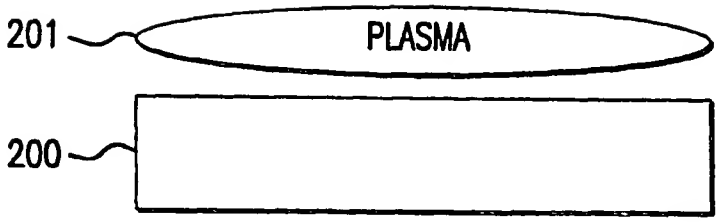


FIG.2A

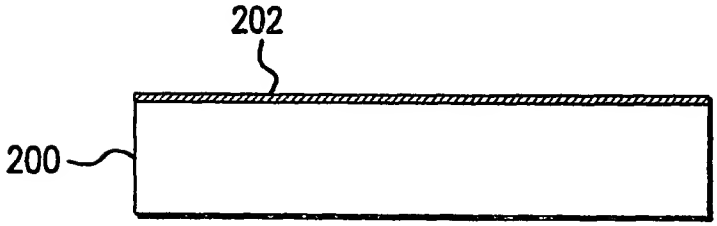


FIG.2B

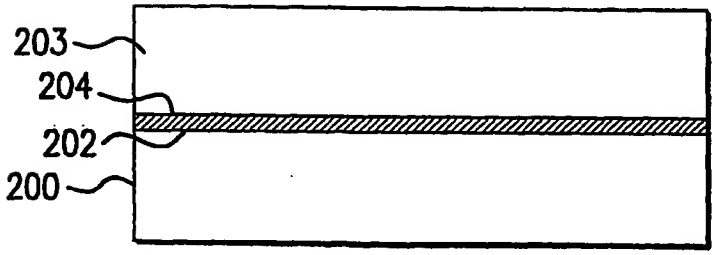


FIG.2C

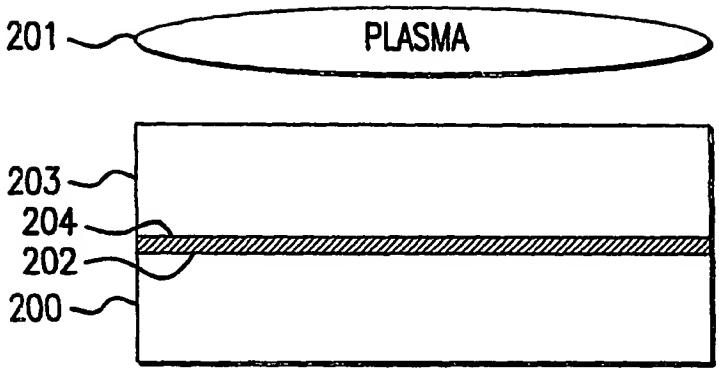


FIG.2D

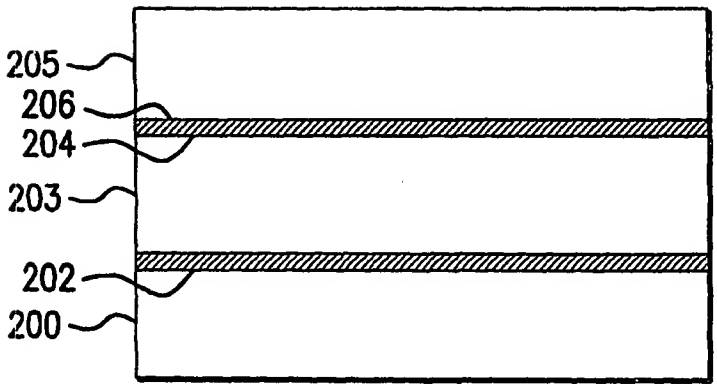


FIG.2E

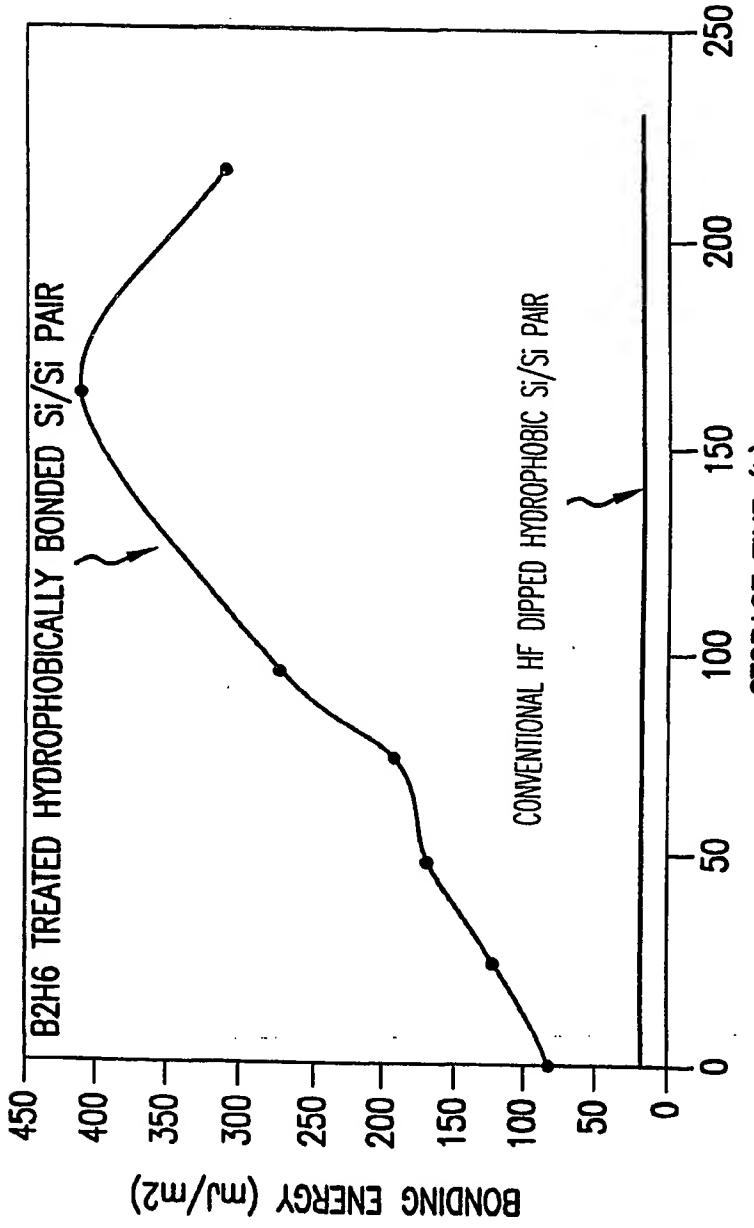

BONDING ENERGY (mJ/m2)
450
400
350
300
250
200
150
100
50
0
0
50
100
150
200
250
STORAGE TIME (h)
B2H6 TREATED HYDROPHOBICALLY BONDED Si/Si PAIR
CONVENTIONAL HF DIPPED HYDROPHOBIC Si/Si PAIR

FIG.3

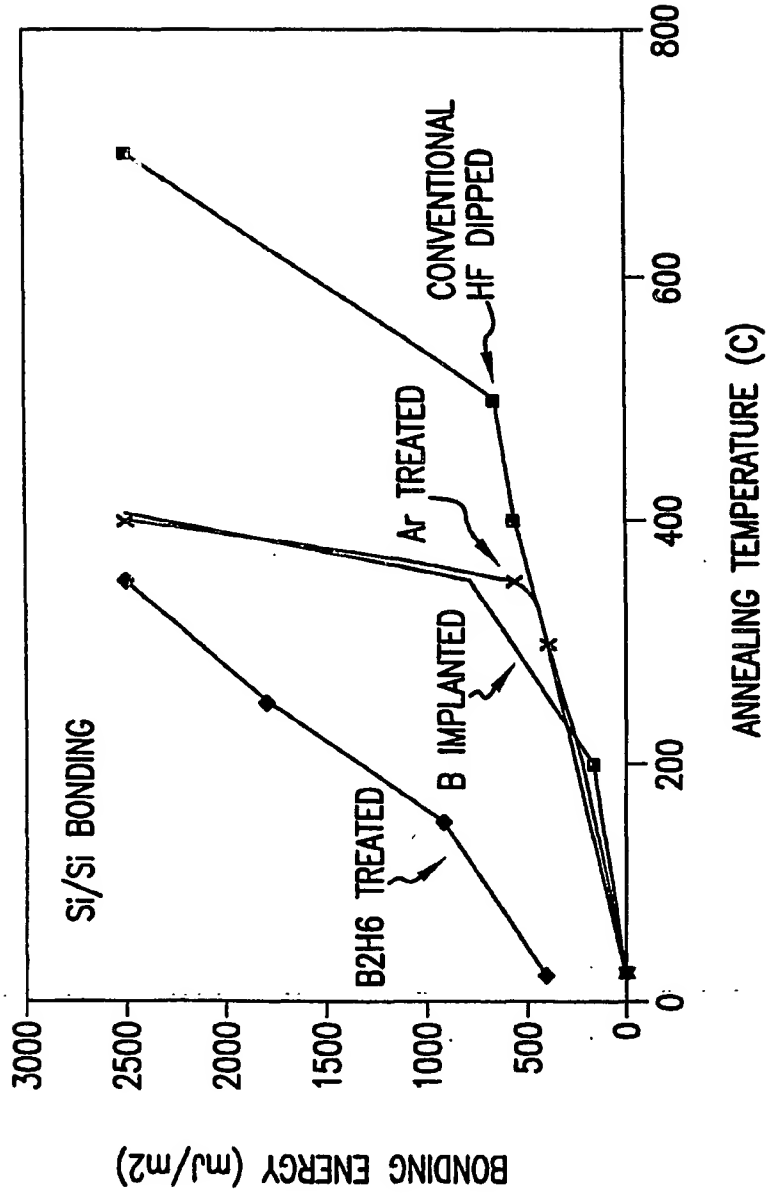

BONDING ENERGY (mJ/m2)
3000
2500
2000
1500
1000
500
0
0
200
400
600
800
ANNEALING TEMPERATURE (C)
Si/Si BONDING
B2H6 TREATED
B IMPLANTED
Ar TREATED
CONVENTIONAL
HF DIPPED

FIG.4

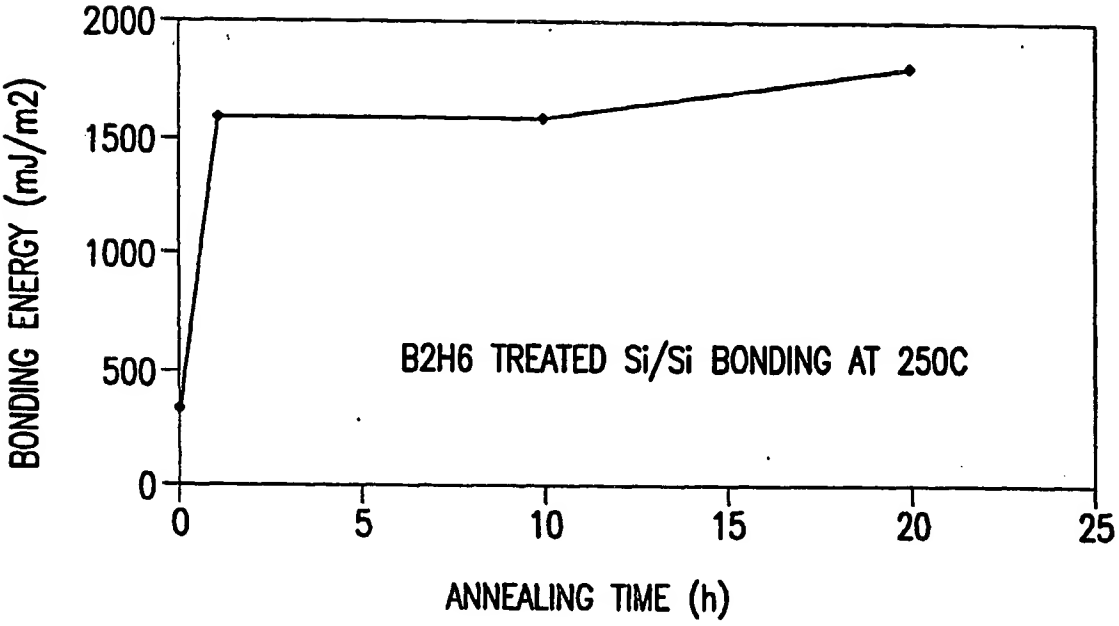

2000
1500
1000
500
0
BONDING ENERGY (mJ/m2)
B2H6 TREATED Si/Si BONDING AT 250C
0
5
10
15
20
25
ANNEALING TIME (h)

FIG.5

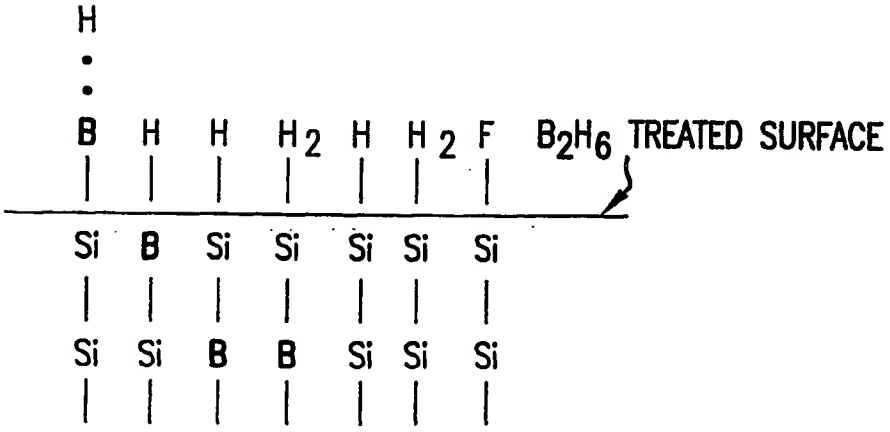

H
B H H H2 H H2 F B2H6 TREATED SURFACE
Si B Si Si Si Si Si
Si Si B B Si Si Si

FIG.6

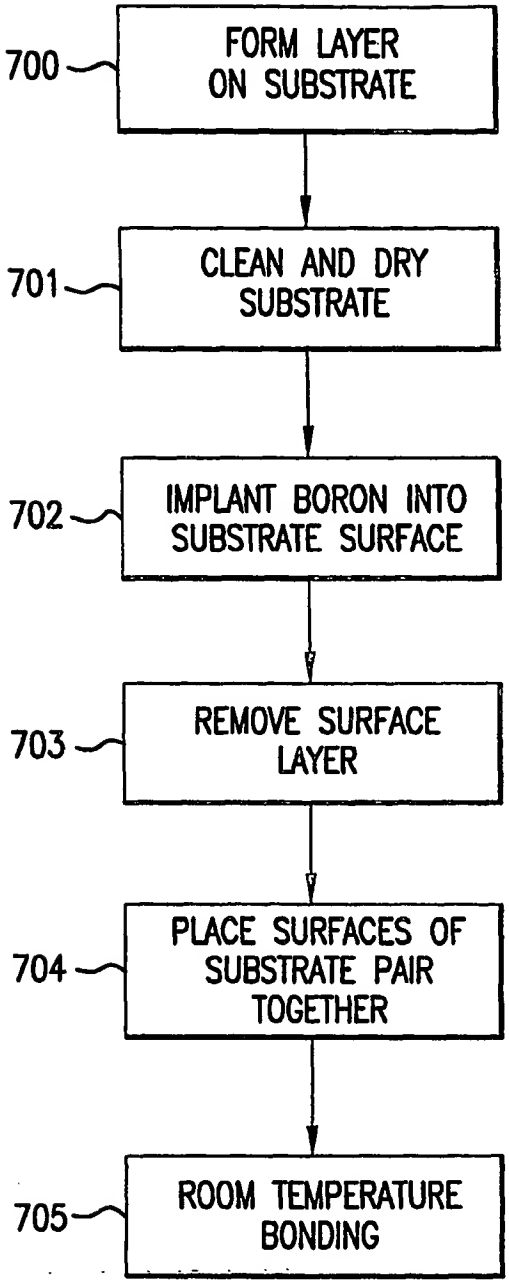

700
FORM LAYER ON SUBSTRATE
701
CLEAN AND DRY SUBSTRATE
702
IMPLANT BORON INTO SUBSTRATE SURFACE
703
REMOVE SURFACE LAYER
704
PLACE SURFACES OF SUBSTRATE PAIR TOGETHER
705
ROOM TEMPERATURE BONDING

FIG.7

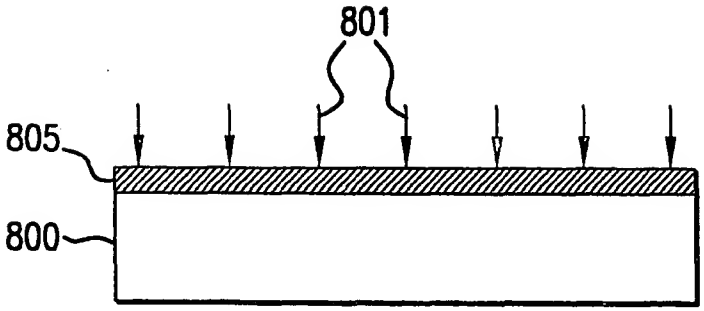


FIG.8A

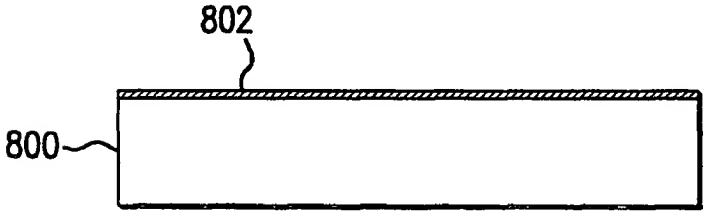


FIG.8B

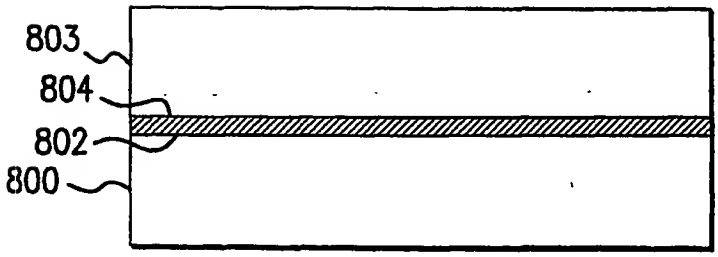


FIG.8C

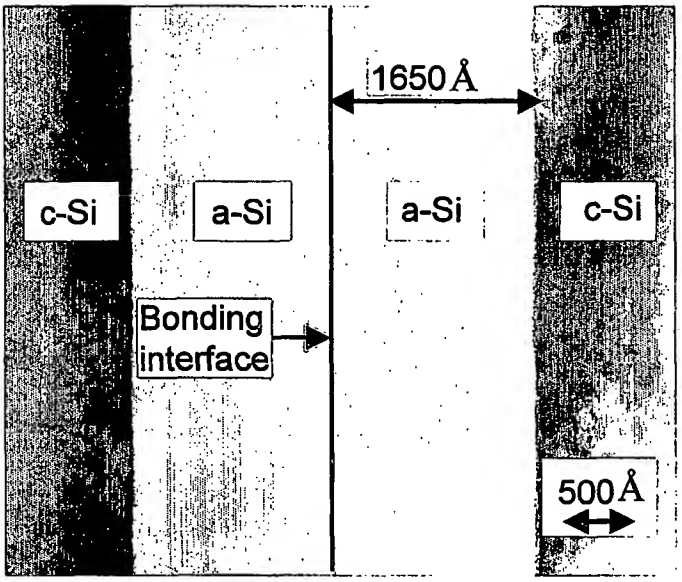


FIG.10

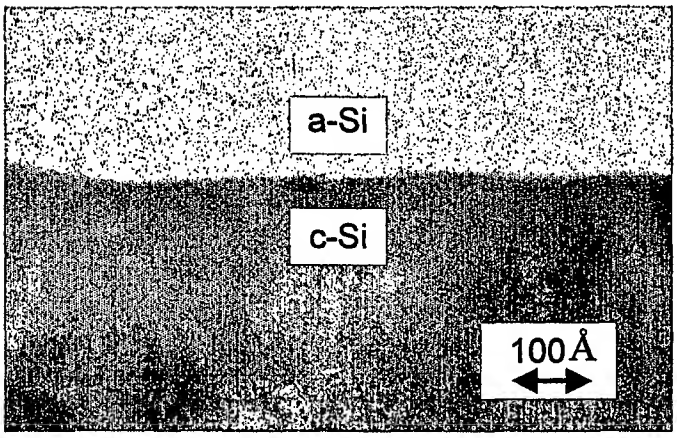


FIG.11

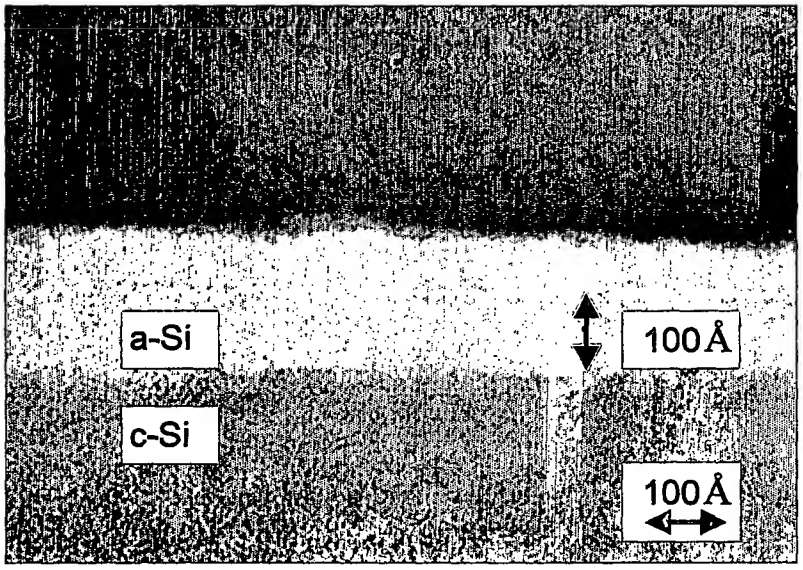


FIG.12

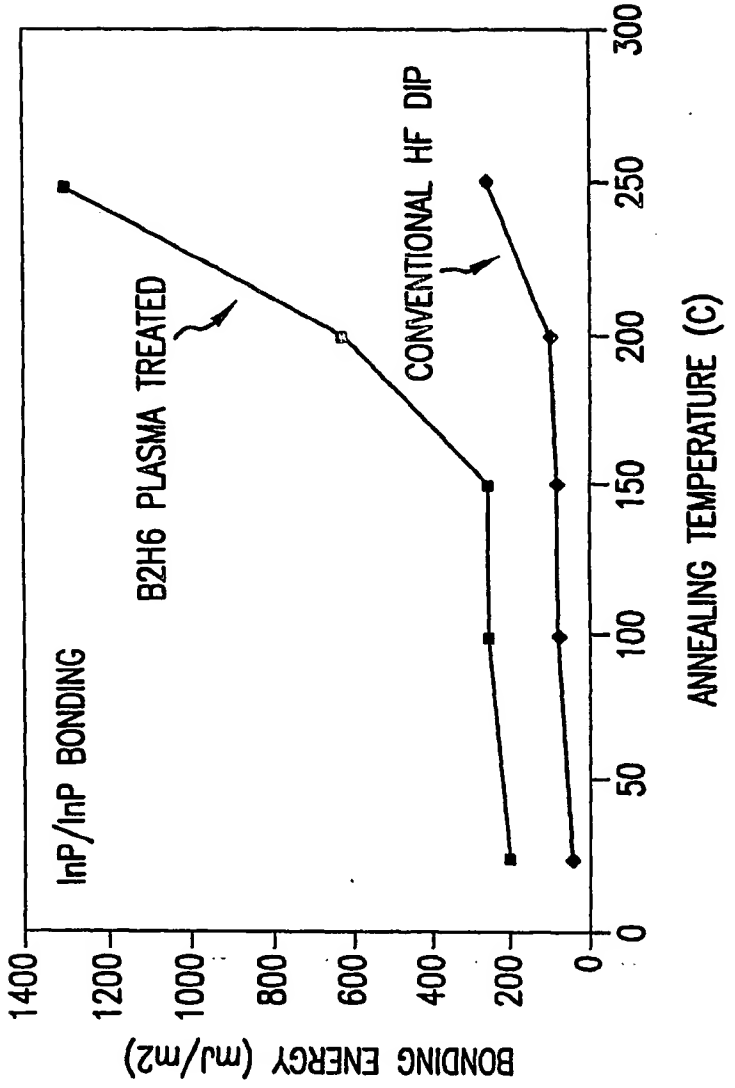

InP/InP BONDING
B2H6 PLASMA TREATED
CONVENTIONAL HF DIP
BONDING ENERGY (mJ/m2)
ANNEALING TEMPERATURE (C)
0
200
400
600
800
1000
1200
1400
0
50
100
150
200
250
300

FIG.13

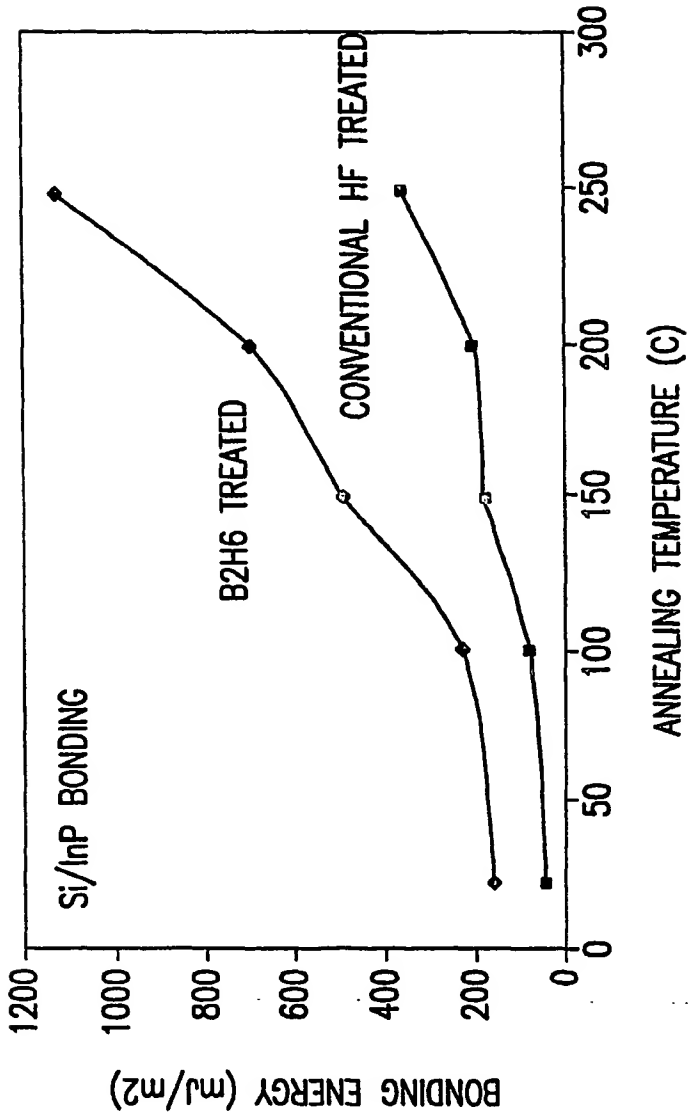

Si/InP BONDING
B2H6 TREATED
CONVENTIONAL HF TREATED
BONDING ENERGY (mJ/m2)
ANNEALING TEMPERATURE (C)
0
200
400
600
800
1000
1200
0
50
100
150
200
250
300

FIG.14

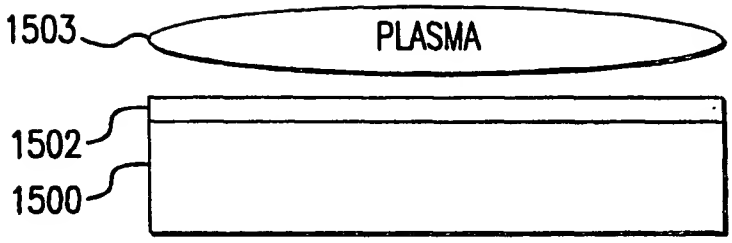


FIG.15A

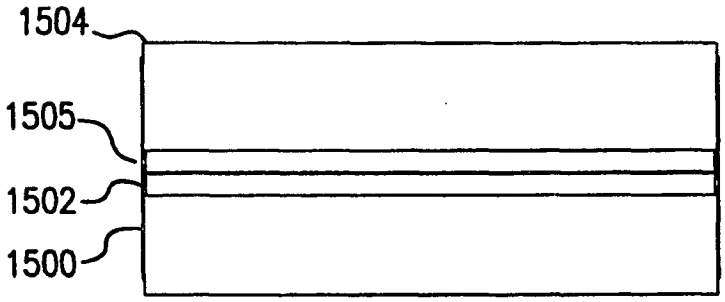
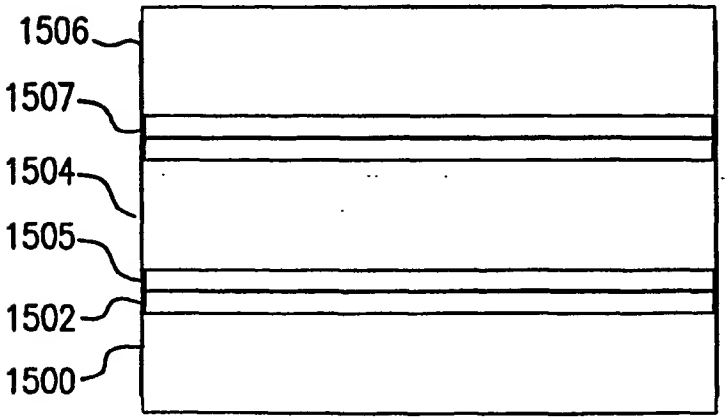


FIG.15B



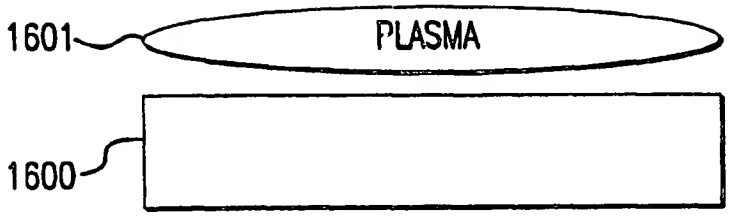


FIG.16A

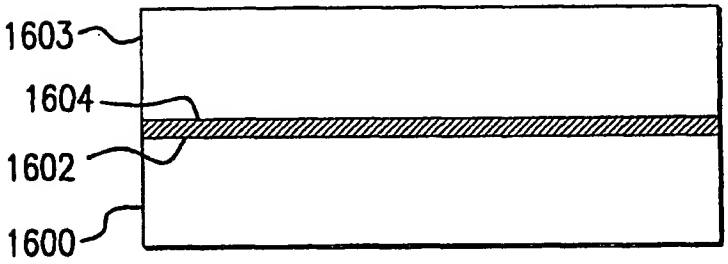


FIG.16B

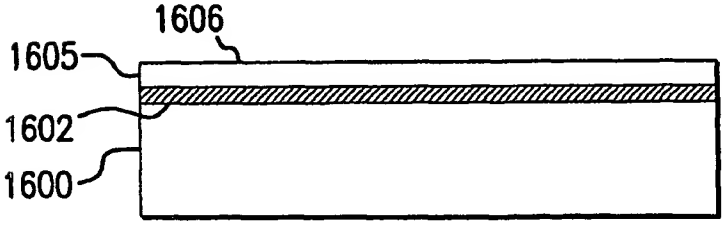


FIG.16C

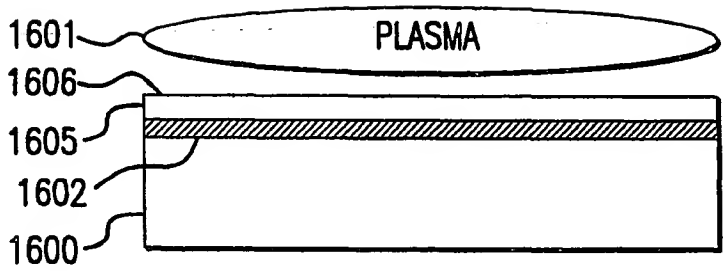


FIG.16D

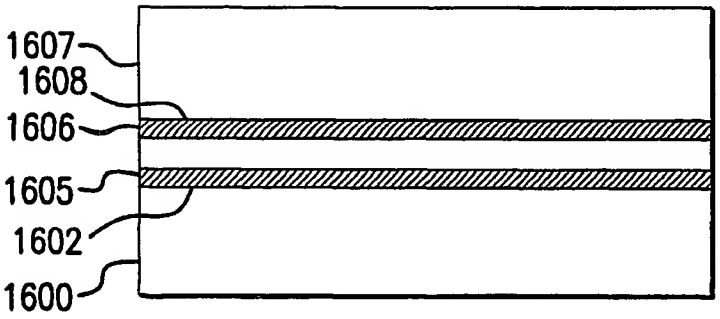


FIG.16E

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/22591

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 21/30, 21/46, 29/04, 31/036, 27/01, 23/48, 23/52, 29/40
US CL : 438/456, 457, 458, 459; 257/52, 64, 65, 66, 347, 756, 757, 758, 759, 760, 782

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 438/456, 457, 458, 459; 257/52, 64, 65, 66, 347, 756, 757, 758, 759, 760, 782

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,783,477 A (KISH, Jr. et al.) 21 July 1998 (21.07.1998), Figure 9.	1-58
Y	US 4,963,505 (FUJII et al.) 16 October 1990 (16.10.1990), column 8, lines 61-65.	1-58
Y,E	US 6,246,068 B1 (SATO et al.) 12 June 2001 (12.06.2001); abstract.	1-58
A,E	US 6,255,731 B1 (OHMI et al.) 03 July 2001 (03.07.2001), Figures 1A-1I.	1-58
A,E	US 6,143,628 A (SATO et al.) 07 November 2000 (07.11.2000), Figures 2A-2C.	1-58
A,E	US 6,120,917 A (EDA) 19 September 2000 (19.09.2000), Figure 22.	1-58

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 September 2001 (26.09.2001)	05 DEC 2001
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Eddie C. Lee Telephone No. (703) 308-0956

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